



FIG. 1

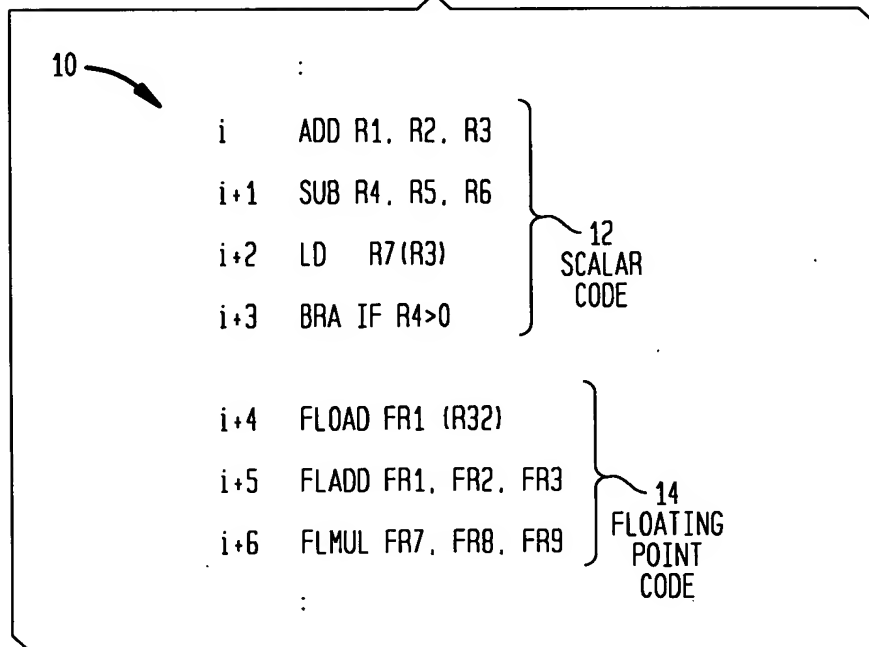
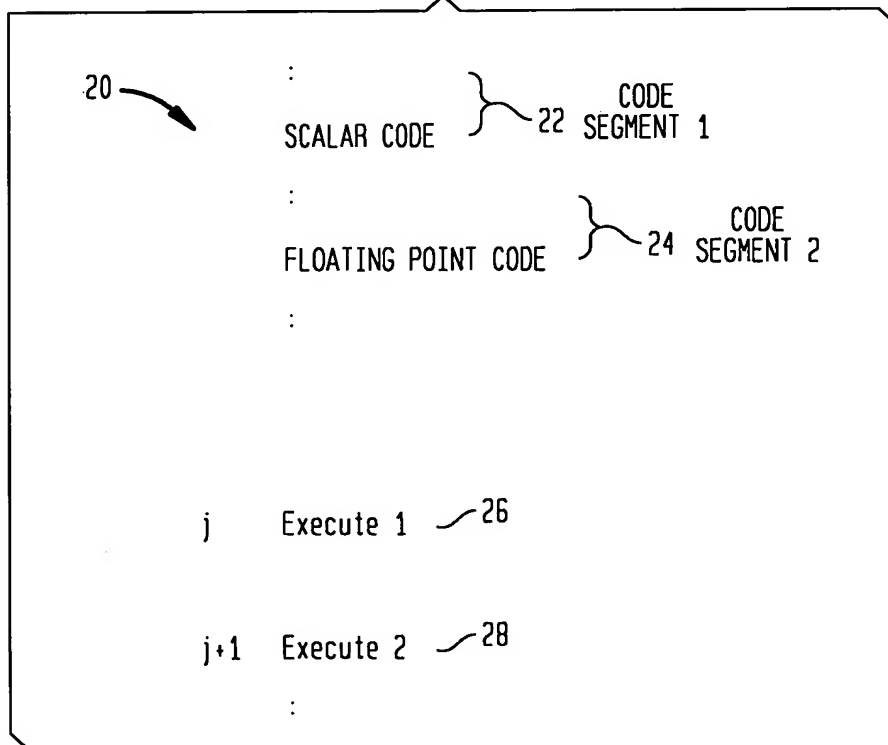


FIG. 2



[illegible]

FIG. 4A

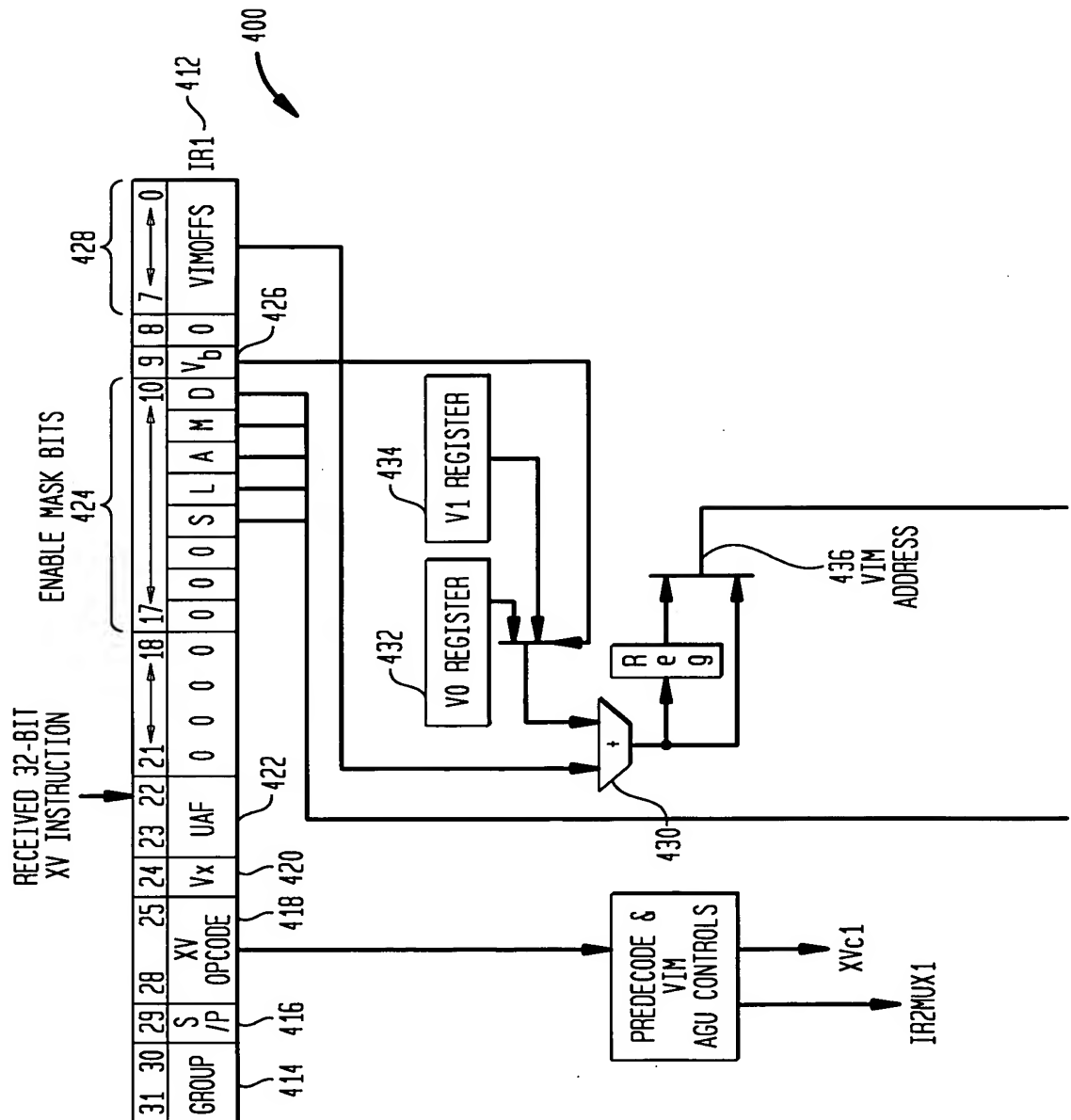


FIG. 4B

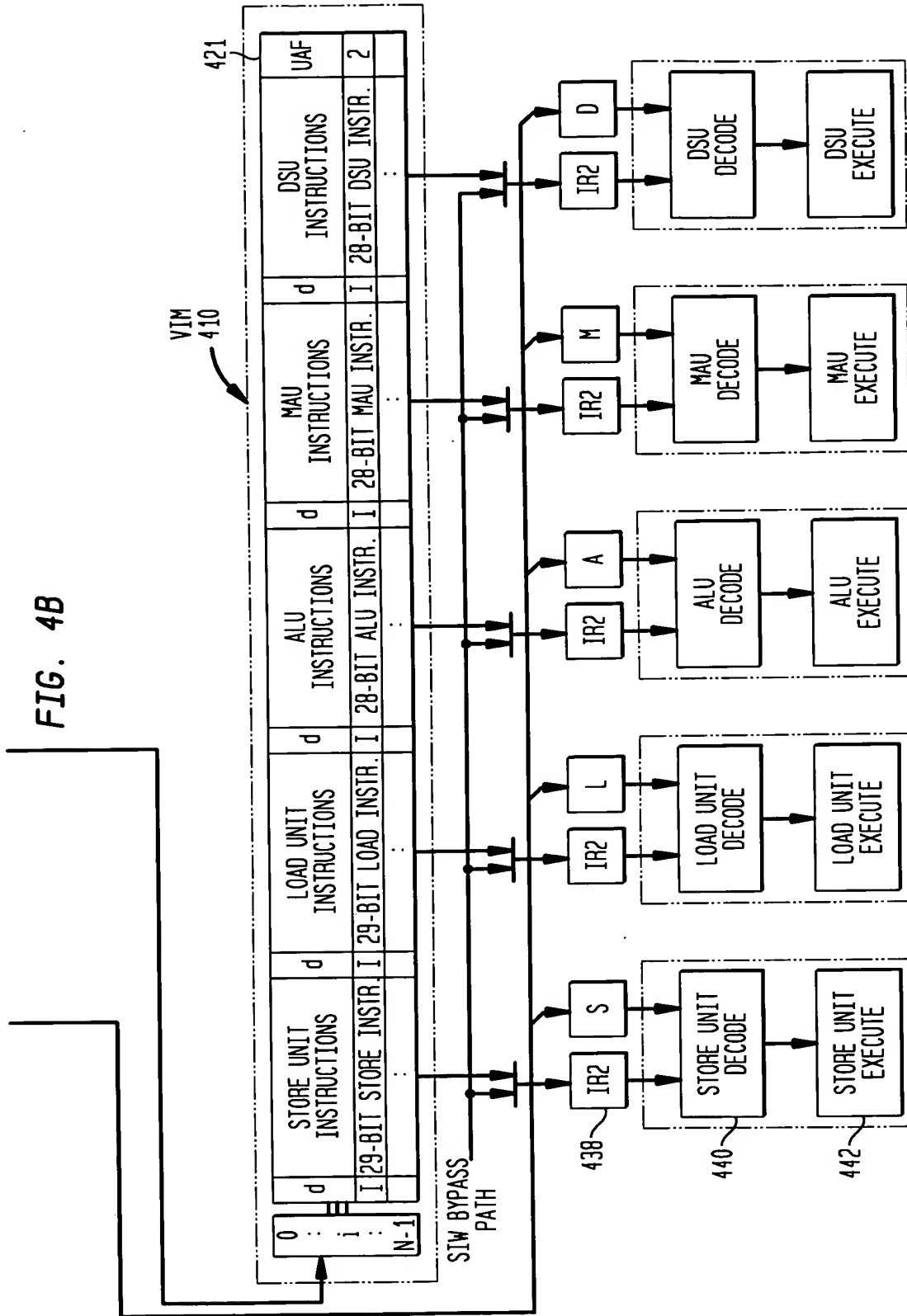
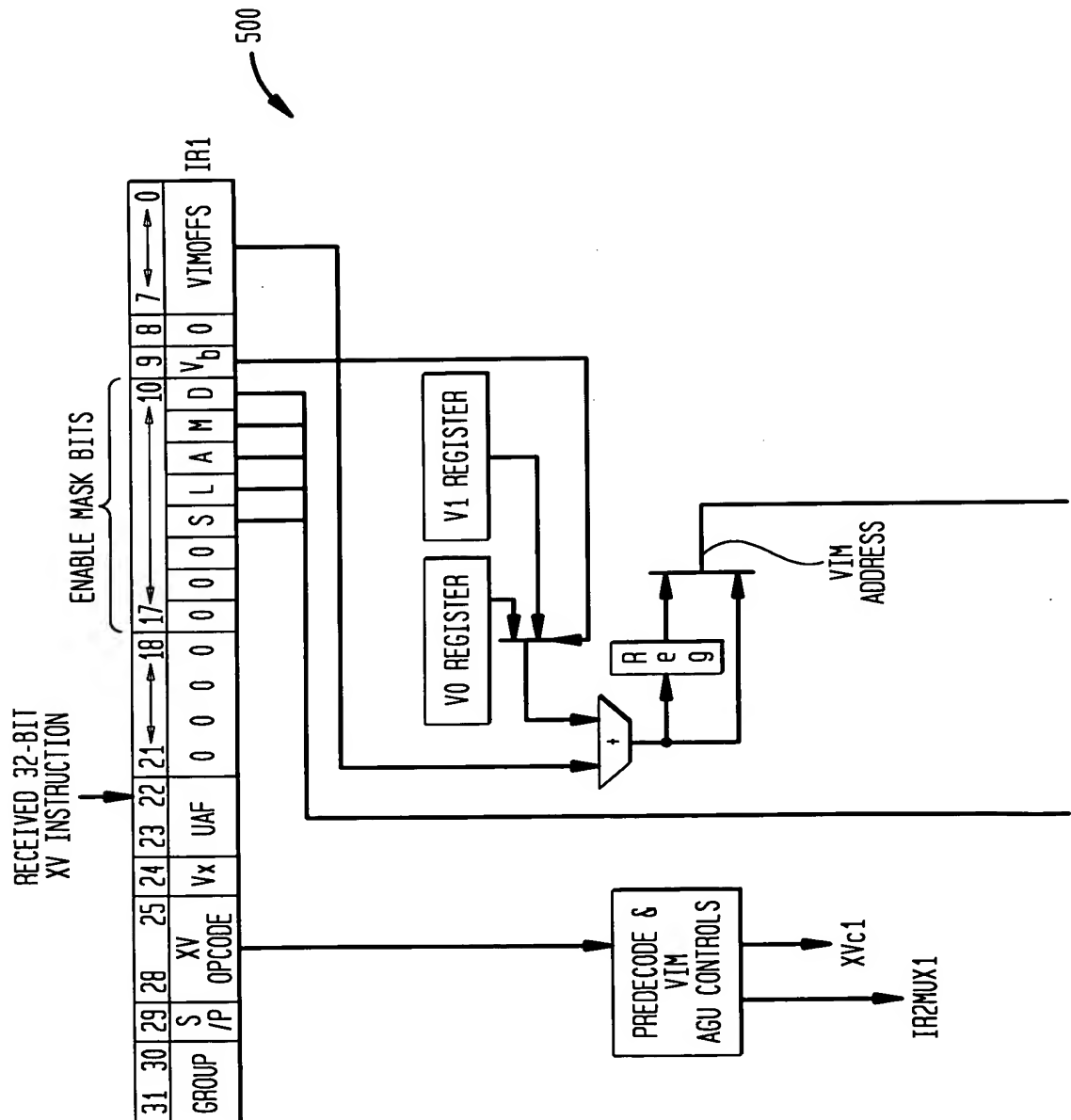


FIG. 5A



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FIG. 5B

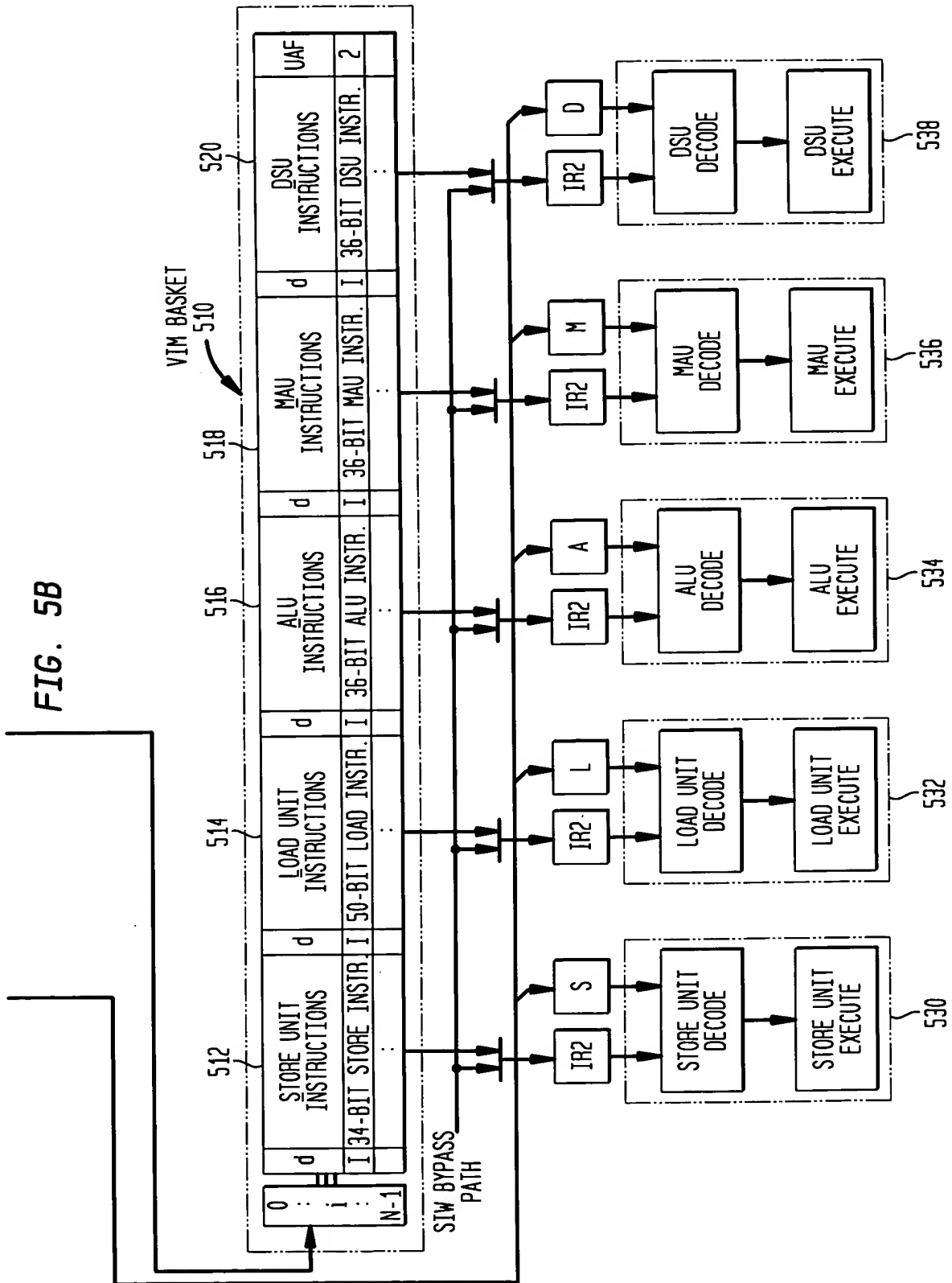


FIG. 6A
(PRIOR ART)

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FIG. 7A

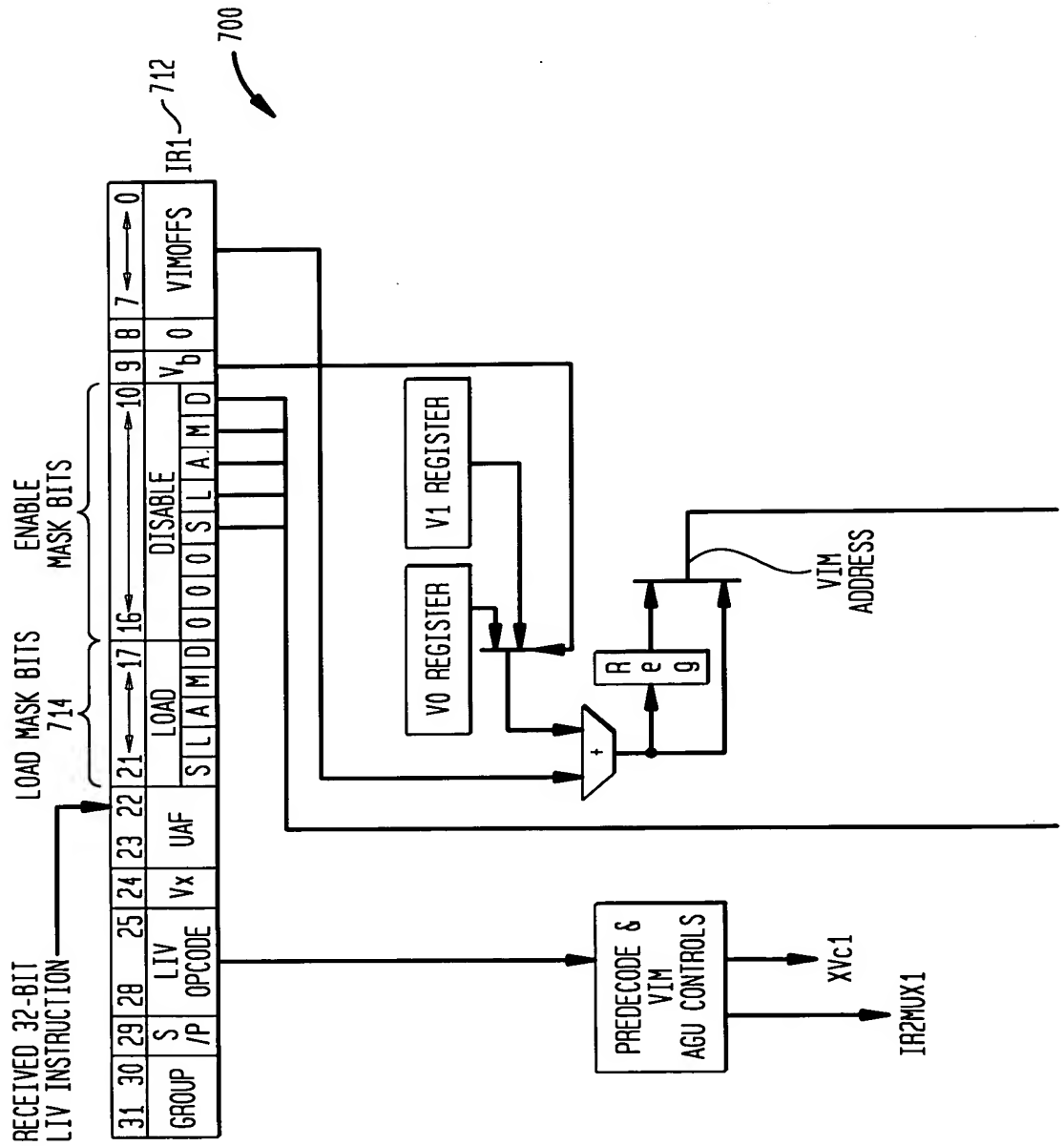
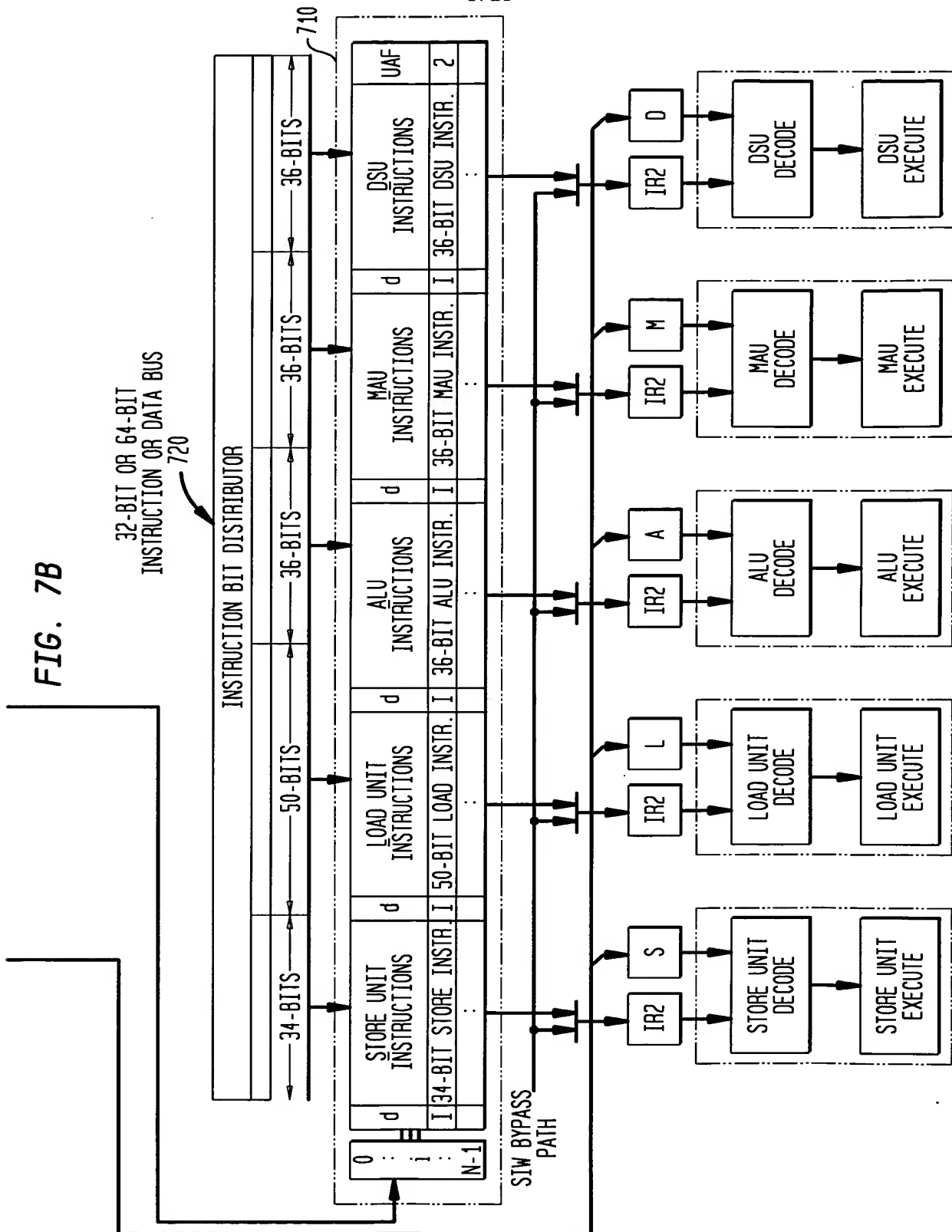
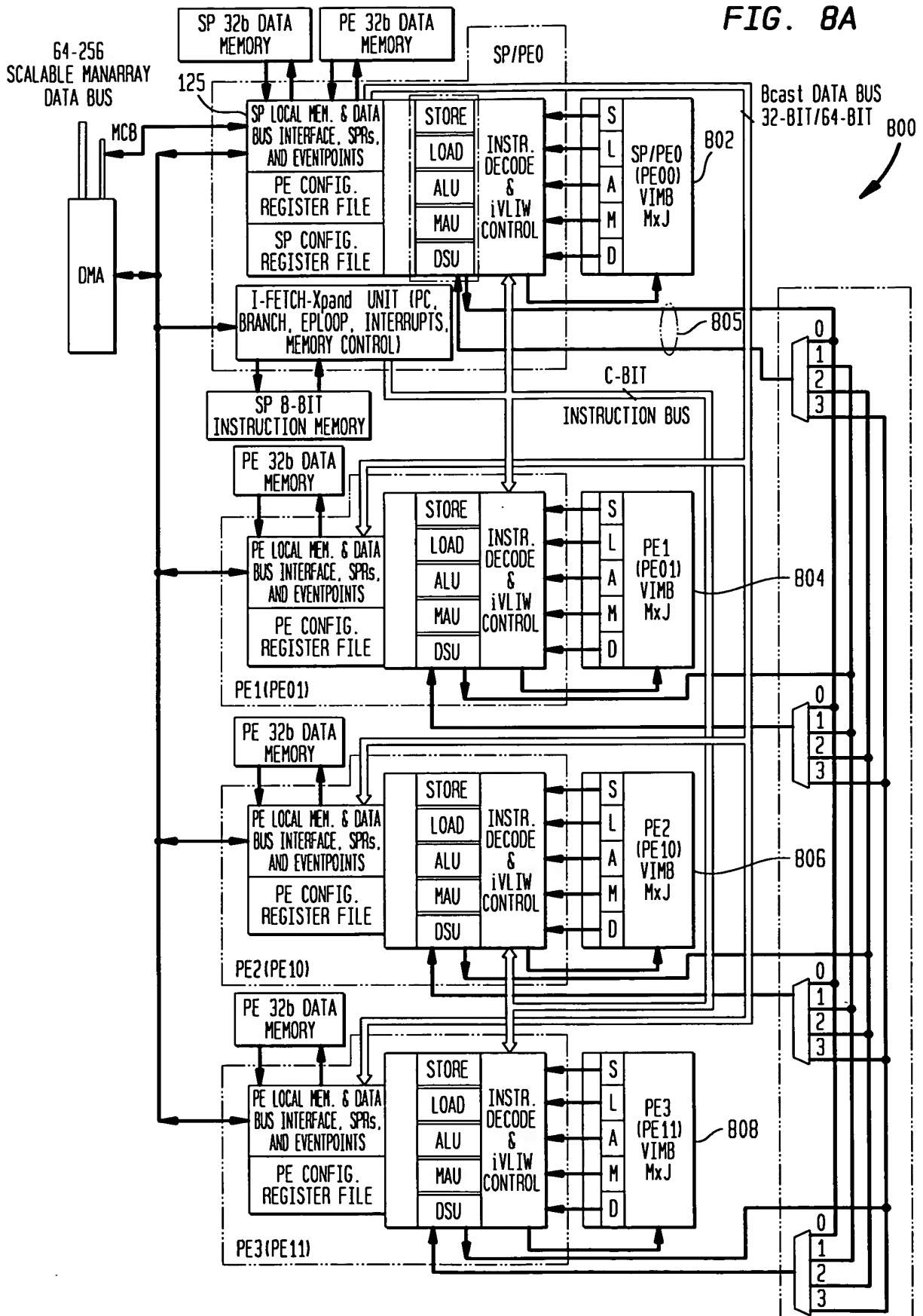


FIG. 7B



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FIG. 8A



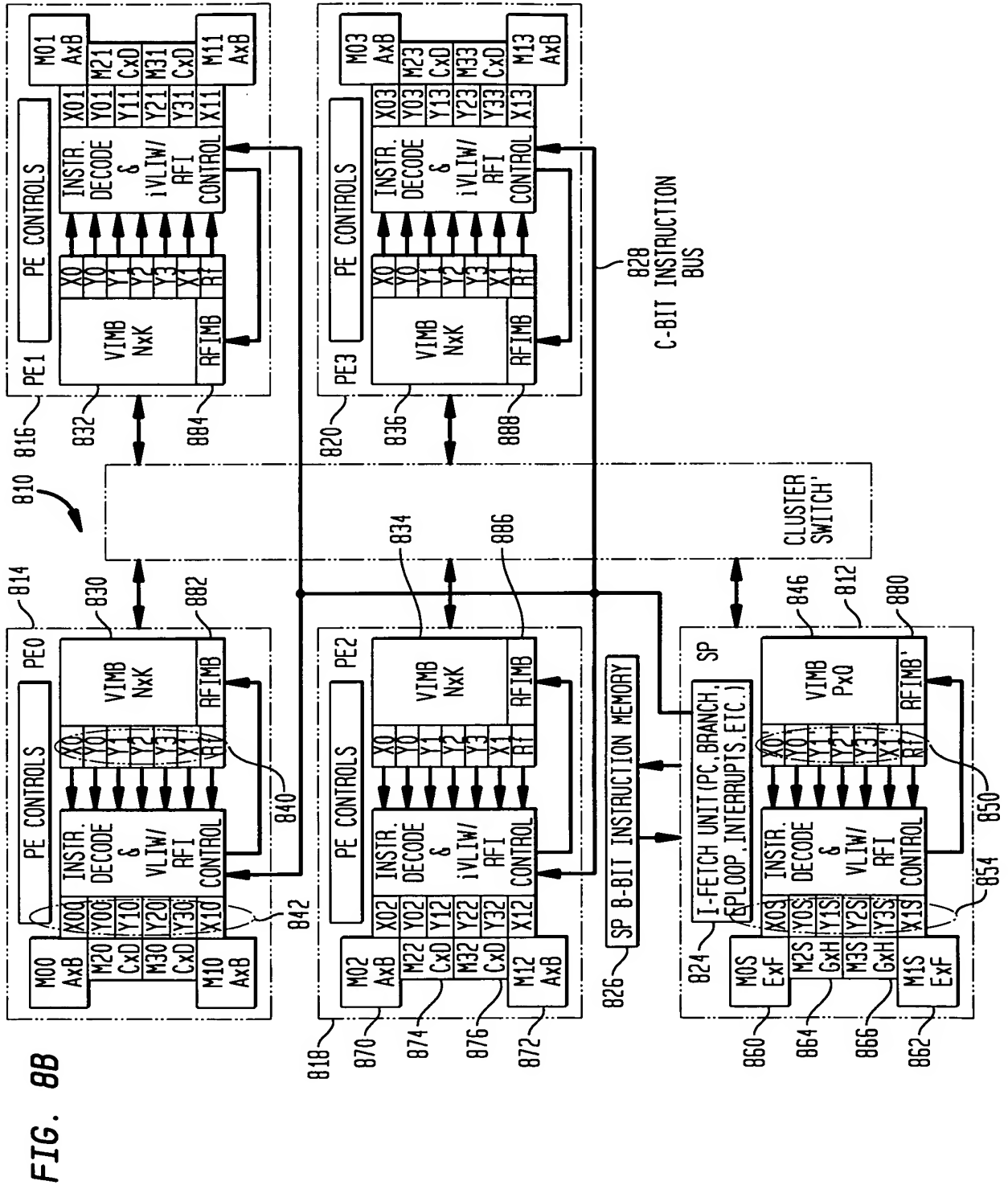


FIG. 9A

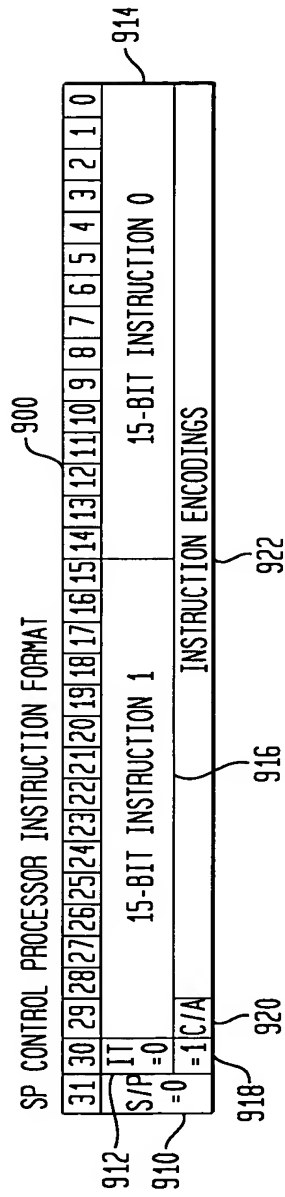


FIG. 9B

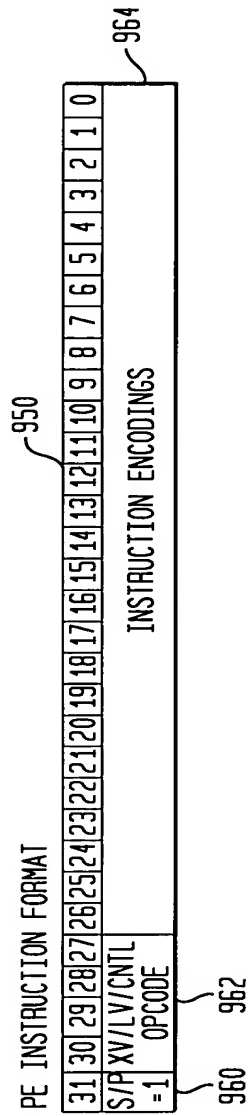


FIG. 10A

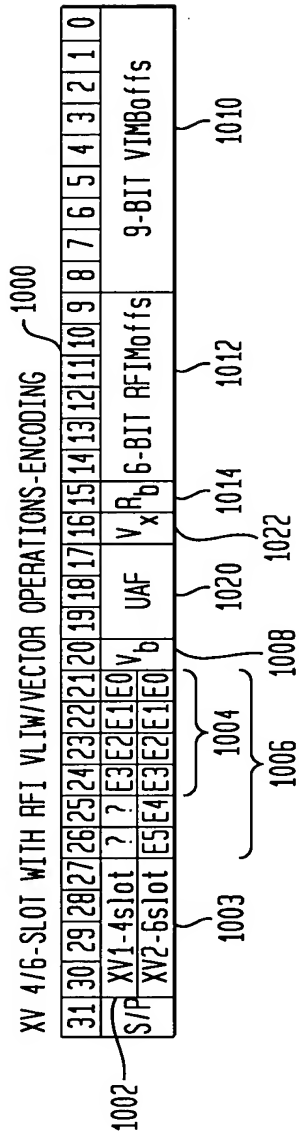


FIG. 10B

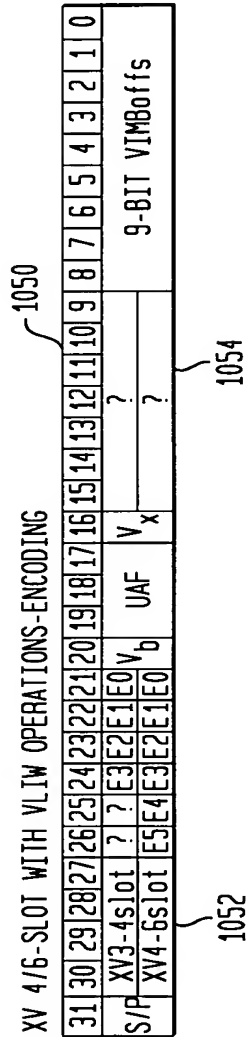


FIG. 11A

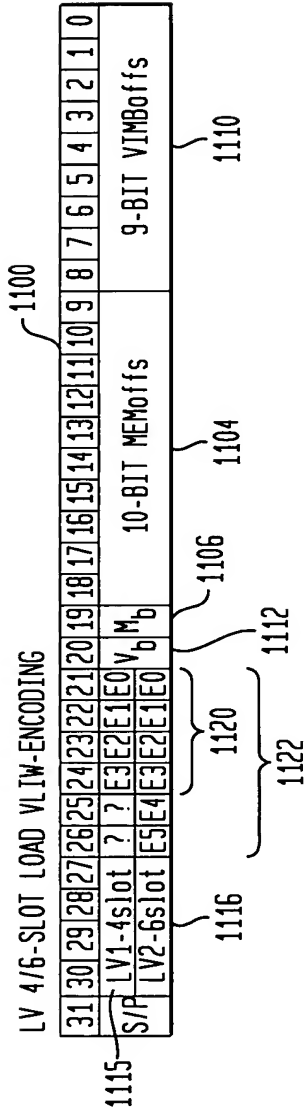


FIG. 11B

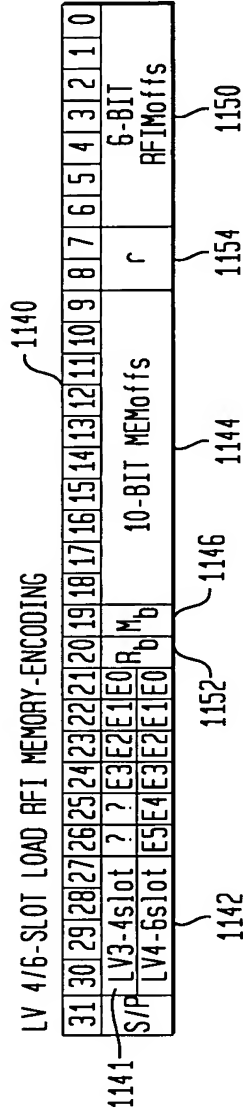
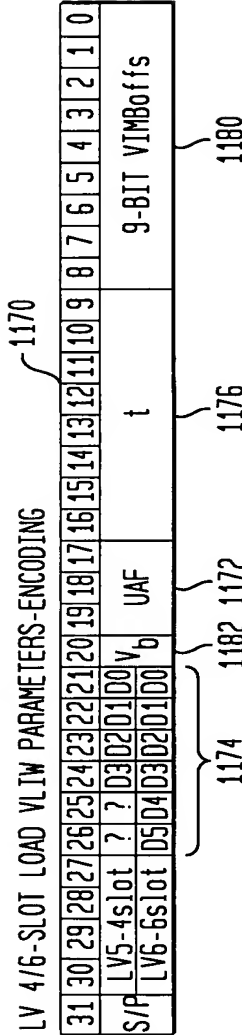


FIG. 11C



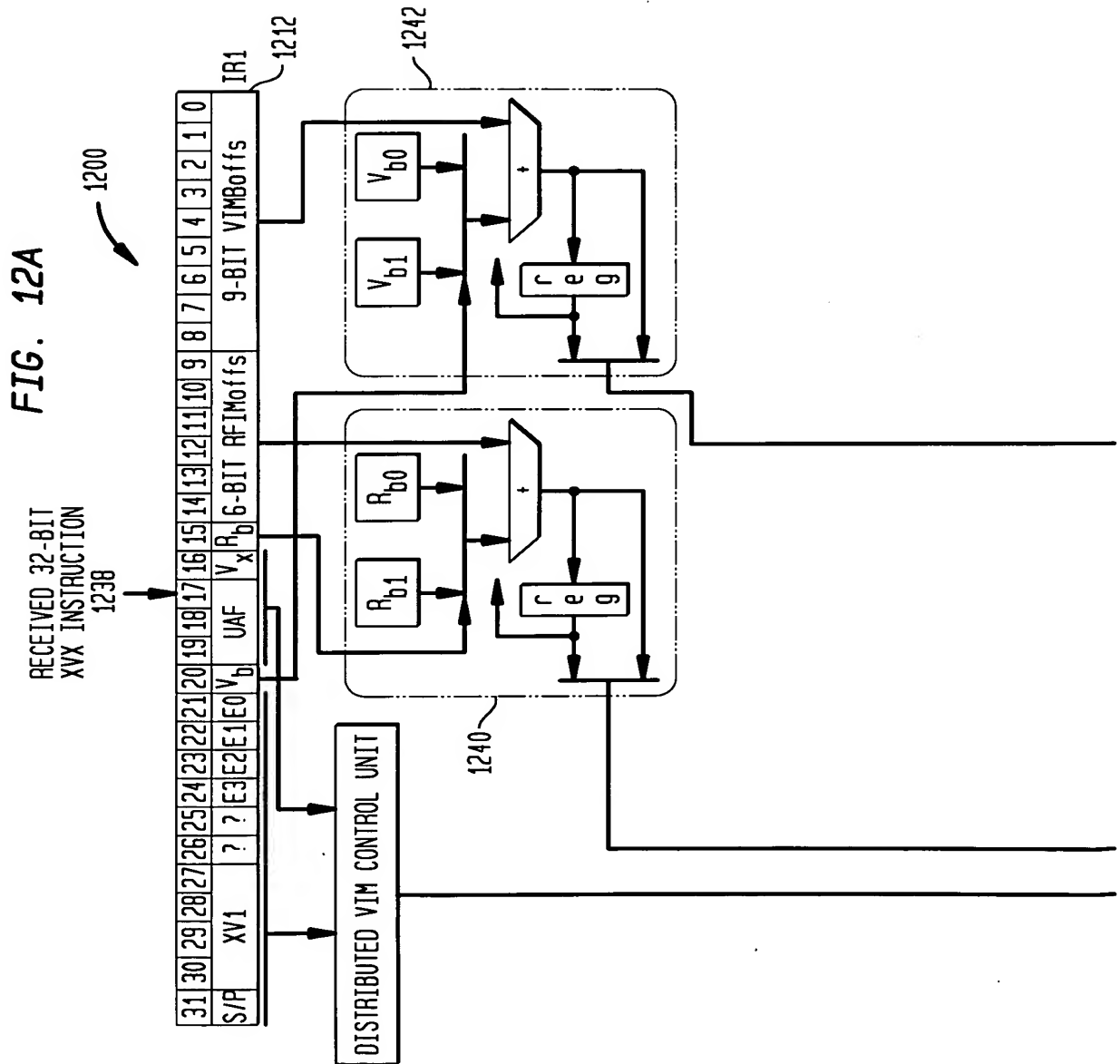
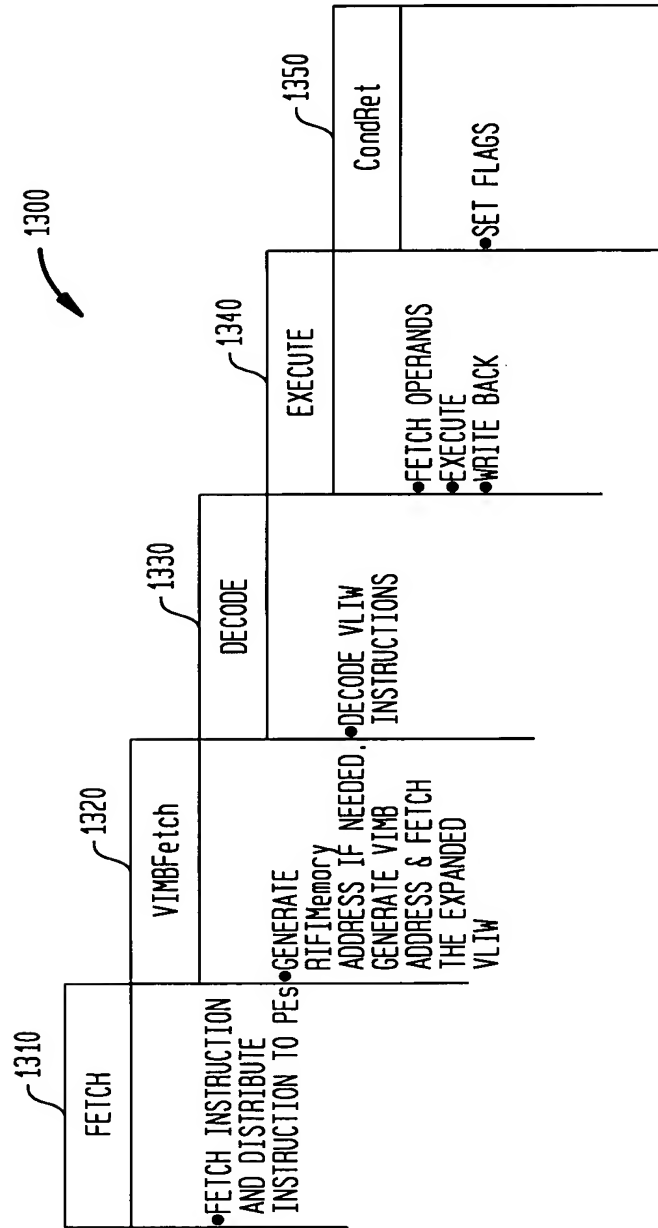
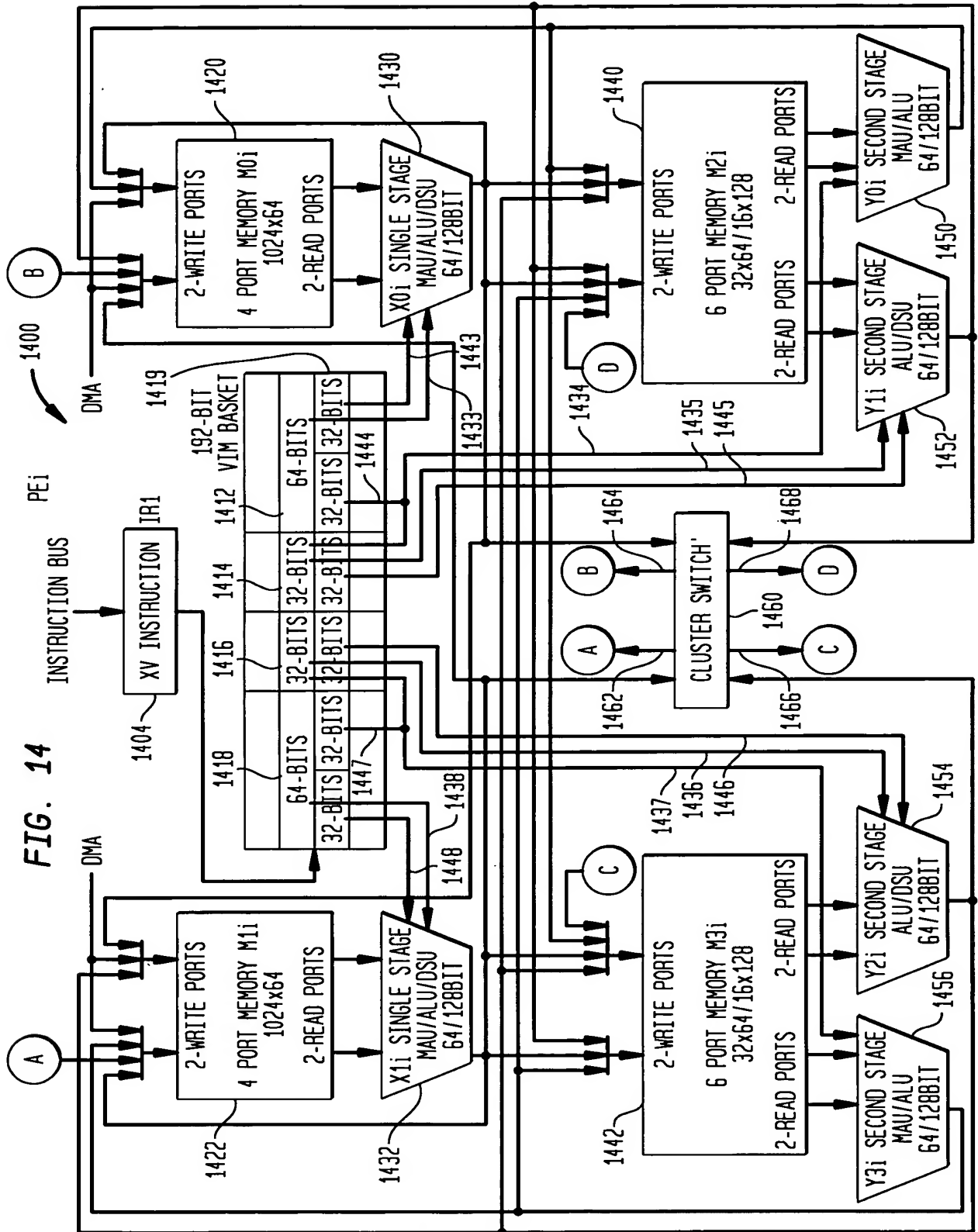


FIG. 13



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FIG. 15

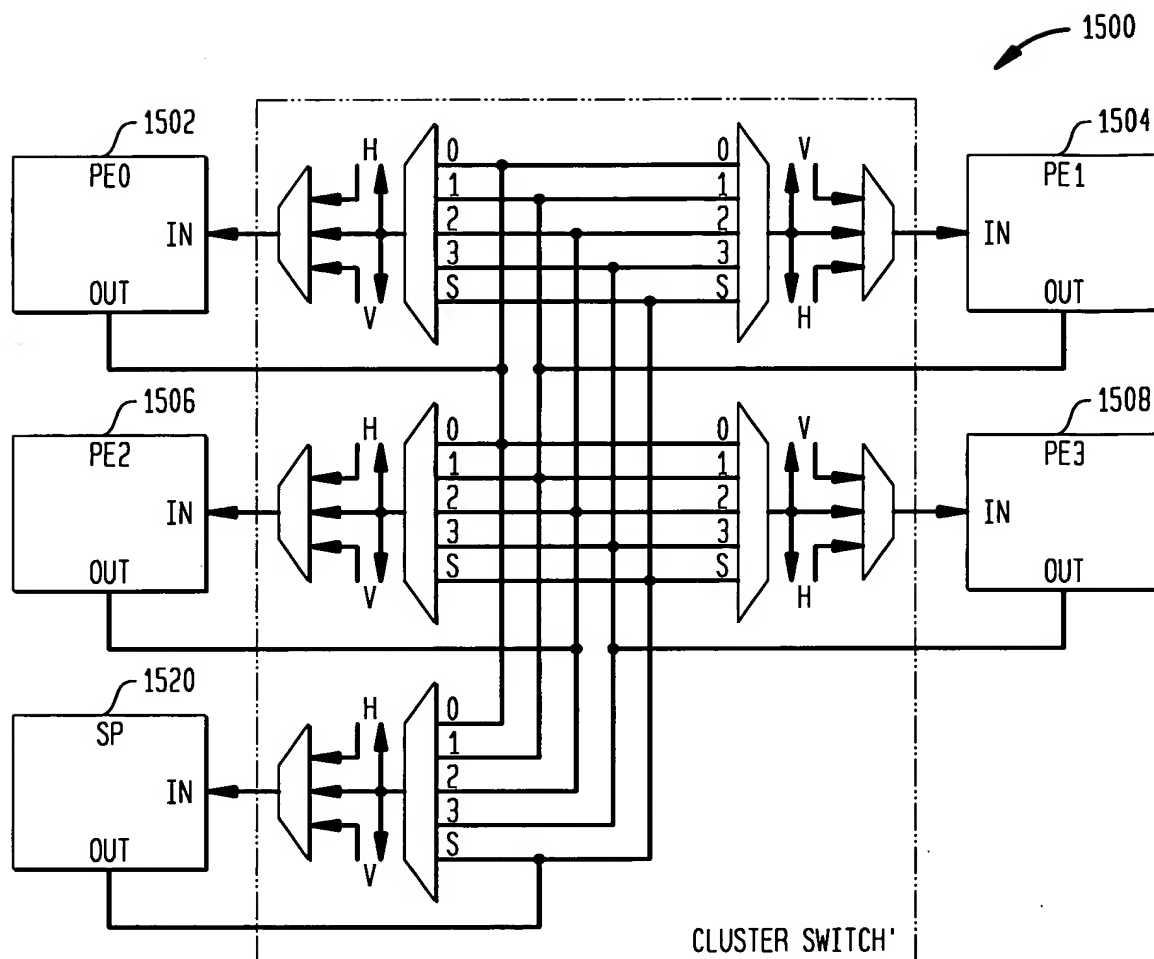


FIG. 16

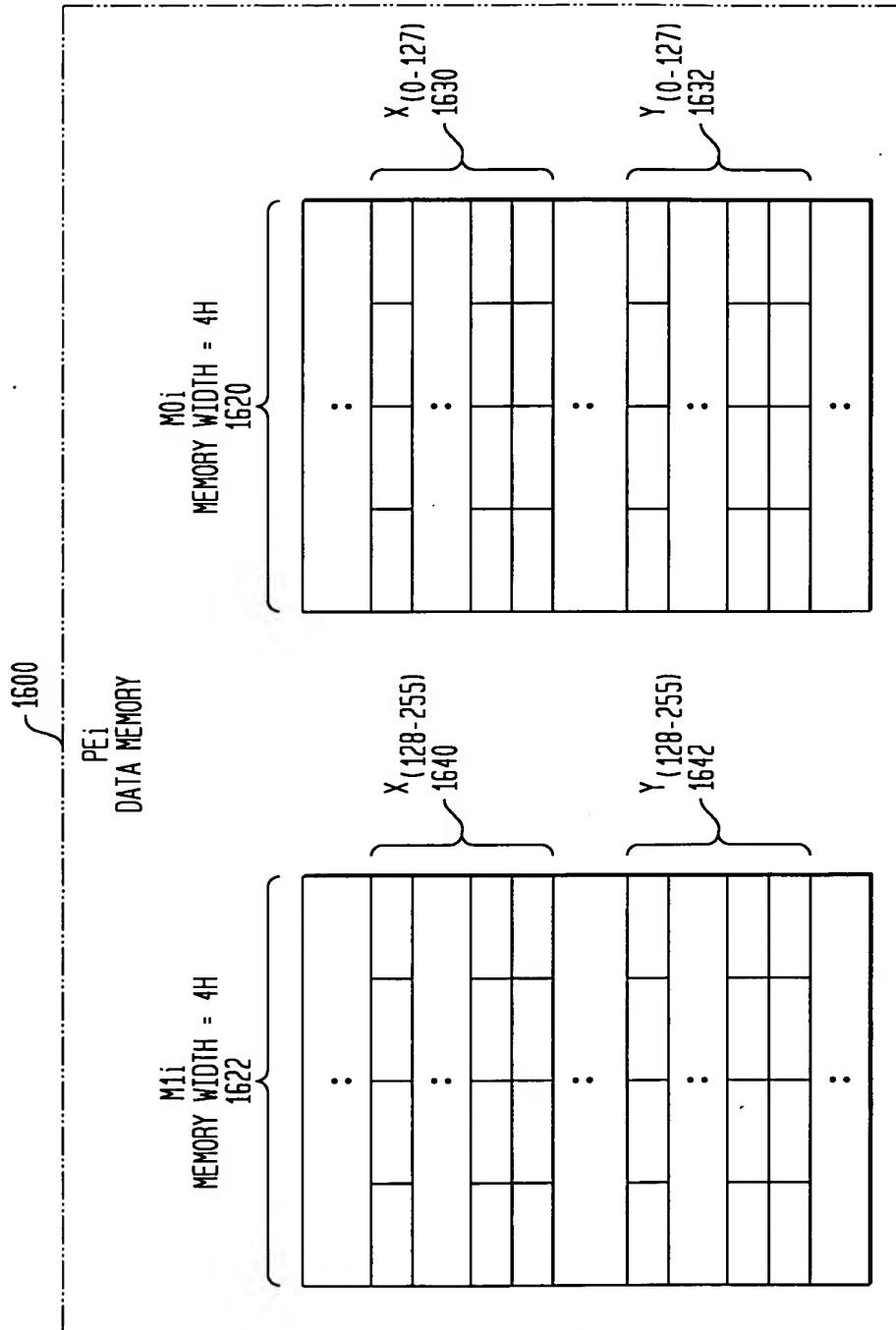


FIG. 17

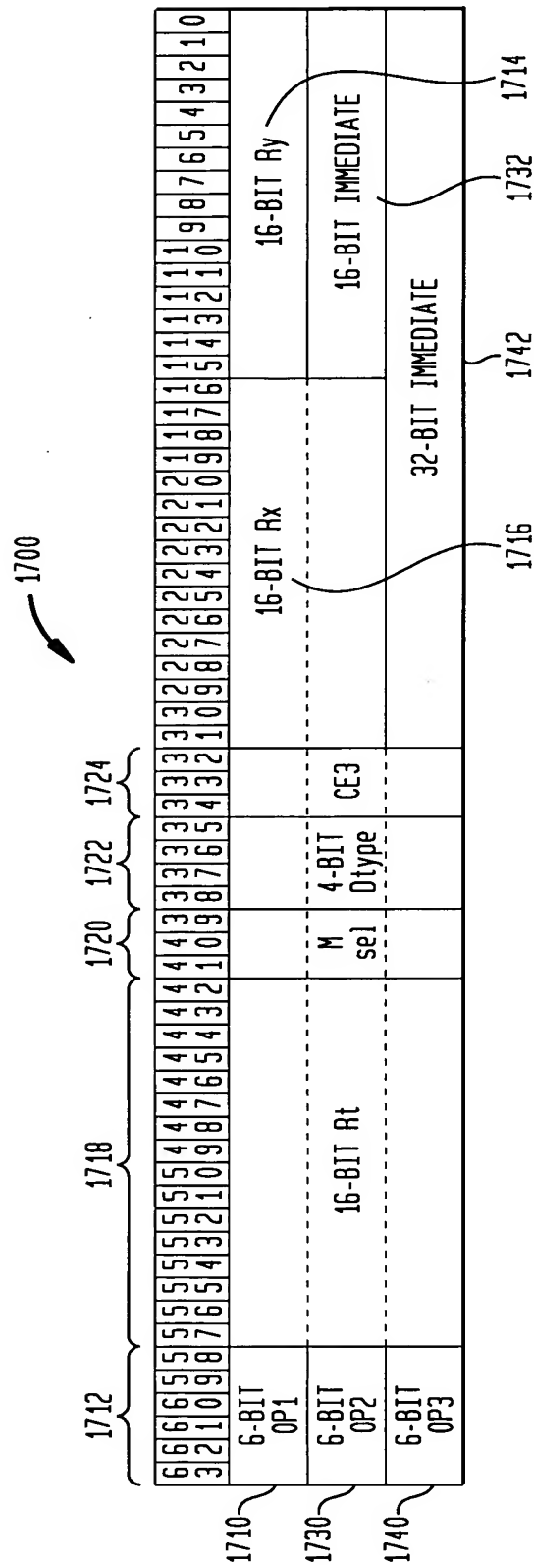


Figure 1 illustrates a parallel multiplier 1800. The multiplier is divided into two main sections, 1810 and 1812, each processing a 4-bit input (X0i, X1i and X0, X1). These inputs are multiplied by 4-bit inputs (Y0i, Y1i and Y0, Y1) to produce 8-bit products (X0i*Y0i, X1i*Y1i). The products are then added to the previous stage's results to produce the final 8-bit output (A0, A1, A2, A3, A4, A5, A6, A7).

FIG. 19

